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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,812	08/20/2002	Dong-Bo Hao		7772

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EXAMINER	
BONURA, TIMOTHY M	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,812	HAO ET AL.	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

- Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington, et al, U.S. Patent Number 6,775,192 and further in view of Miner, U.S. Patent Number 6,862,704.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington, et al, U.S. Patent Number 6,775,192 and further in view of Miner, U.S. Patent Number 6,862,704.

3. Regarding claim 1:

a. Regarding the limitation of "a command translation unit, coupled to the computer main board through a standard interface for receiving and translation a write-in data from a specified port address and latching up the translated write-in data," Harrington discloses a system with a DRDRAM which is connected to a memory device to check power operational states of specific address in memory. (Lines 57-65 of Column 2). Harrington also discloses that any connector capable of receiving a signal for test can be used to connect the tester to the memory. (Lines 40-48 of Column 5, see also Figure 2).

b. Regarding the limitation of "a test procedure control unit, coupled to the command translation unit and the computer main board for issuing test control commands according to a preset testing procedure and reading the latched write-in data inside the command translation unit so that functionality of the computer main board is

assessed and results are registered," Harrington discloses a system in which DRDRAM issues test commands based on stored readable instructions (Lines 25-30 of Column 6). Harrington also discloses that test results are gathered and analyzed by the DRDRAM during testing. (Lines 38-60 of Column 7 and Lines 55-60 of Column 8). Harrington does not disclose a test procedure control unit that can latch write-in data inside the computer main board. Miners discloses a system with a test management logic that accepts test parameter in a configuration register and are transferred from the test controller over the test control bus. (Lines 18-20 of Column 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power test circuitry of Harrington with the BIST of Miner. One of ordinary skill would have been inclined because Harrington discloses the need of and external memory-testing device for storing testing procedures. (Lines 5-18 of Column 6). Miner discloses this test management logic external to the system to fulfill the stated need of Harrington. (See Miner figure 5).

4. Regarding claim 2, Miner discloses a system with means to display and analysis results from test commands. (Lines 53-60 of Column 11).

5. Regarding claim 3, Harrington discloses a system wherein test instructions can be stored and selected from 3 CAL commands. (Lines 58-60 of Column 6).

6. Regarding claim 4, Harrington discloses a system wherein a Standby/reduced power state is tested. (Lines 4-6 of Column 3 and Lines 57-60 of Column 7).

7. Regarding claim 5, Miner discloses a system with means to display test commands configurations for an operator to configure. (Lines 30-34 of Column 12).

8. Regarding claim 6, Harrington discloses a system wherein a Standby/reduced power state is tested. (Lines 4-6 of Column 3 and Lines 57-60 of Column 7). Harrington discloses that the system can enter a standby state via a command. (Lines 45-47 of Column 6).

9. Regarding claim 7, Miner discloses a system in which the number of repetitions of a test procedure is programmable. (Lines 35-45 of Column 10).

10. Regarding claim 8, Harrington discloses a system wherein the testing instructions can be stored in ROM. (Lines 30-32 of Column 6).

11. Regarding claim 9:

c. Regarding the limitation of "a computer main board testing device connected to a standard interface on the computer main board, wherein the testing device controls the switching and resetting of the computer main board so that test control commands are sequentially transmitted according to preset testing procedures," Miners discloses a system with a test management logic that accepts test parameter in a configuration register and are transferred from the test controller over the test control bus. (Lines 18-20 of Column 11). Miner does not disclose a system with a power test procedure. Harrington discloses a system with a DRDRAM, which is connected to a memory device to check power operational states of specific address in memory. (Lines 57-65 of Column 2). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power test circuitry of Harrington with the BIST of Miner. One of ordinary skill would have been inclined because Harrington discloses the need of and external memory-testing device for storing testing procedures. (Lines 5-18 of Column 6). Miner discloses this test management logic external to the system to fulfill the stated need of Harrington. (See Miner figure 5).

d. Regarding the limitation of "a computer main board," Miner discloses a microprocessor. (Lines 55-57 of Column 11, see Figure 5).

12. Regarding claim 10, Miner discloses a system with means to display and analysis results from test commands. (Lines 53-60 of Column 11).

13. Regarding claim 11, Harrington discloses a system wherein a Standby/reduced power state is tested. (Lines 4-6 of Column 3 and Lines 57-60 of Column 7).

14. Regarding claim 12, Harrington discloses a system wherein a Standby/reduced power state is tested. (Lines 4-6 of Column 3 and Lines 57-60 of Column 7). Harrington discloses that the system can enter a standby state via a command. (Lines 45-47 of Column 6).

15. Regarding claim 13, Harrington also discloses that any connector capable of receiving a signal for test can be used to connect the tester to the memory. (Lines 40-48 of Column 5, see also Figure 2). Harrington also discloses that test results are gathered and analyzed by the DRDRAM during testing. (Lines 38-60 of Column 7 and Lines 55-60 of Column 8).

16. Regarding claim 14, Miner discloses a system that can find errors on a bit-by-bit basis and store those errors. (Lines 48-67 of Column 11).

17. Regarding claim 15:

e. Regarding the limitation of "sequentially issuing test control commands according to a preset testing procedure for controlling the switching and resetting of the computer main board," Harrington discloses a system in which DRDRAM issues test commands based on stored readable instructions (Lines 25-30 of Column 6). Harrington also discloses that test results are gathered and analyzed by the DRDRAM during testing. (Lines 38-60 of Column 7 and Lines 55-60 of Column 8).

f. Regarding the limitation of "retrieving write-in data from a specified port address; translating write-in data through a standard interface on the computer main board so that

functionality of the computer main board is assessed and test results are registered," Harrington discloses a system with a DRDRAM which is connected to a memory device to check power operational states of specific address in memory. (Lines 57-65 of Column 2). Harrington also discloses that any connector capable of receiving a signal for test can be used to connect the tester to the memory. (Lines 40-48 of Column 5, see also Figure 2). Harrington does not disclose a test procedure control unit that can latch write-in data inside the computer main board. Miners discloses a system with a test management logic that accepts test parameter in a configuration register and are transferred from the test controller over the test control bus. (Lines 18-20 of Column 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power test circuitry of Harrington with the BIST of Miner. One of ordinary skill would have been inclined because Harrington discloses the need of and external memory-testing device for storing testing procedures. (Lines 5-18 of Column 6). Miner discloses this test management logic external to the system to fulfill the stated need of Harrington. (See Miner figure 5).

18. Regarding claim 16, Miner discloses a system with means to display and analysis results from test commands. (Lines 53-60 of Column 11).

19. Regarding claim 17, Harrington discloses a system wherein a Standby/reduced power state is tested. (Lines 4-6 of Column 3 and Lines 57-60 of Column 7).

20. Regarding claim 18, Harrington discloses a system wherein a Standby/reduced power state is tested. (Lines 4-6 of Column 3 and Lines 57-60 of Column 7). Harrington discloses that the system can enter a standby state via a command. (Lines 45-47 of Column 6).

21. Regarding claim 19, Miner discloses a system in which the number of repetitions of a test procedure is programmable. (Lines 35-45 of Column 10).

22. Regarding claim 20, Harrington also discloses that any connector capable of receiving a signal for test can be used to connect the tester to the memory. (Lines 40-48 of Column 5, see also Figure 2).

23. Regarding claim 21:

g. Regarding the limitation of "a command translation unit, coupled to the computer main board through a standard interface for receiving and translation a write-in data from a specified port address and latching up the translated write-in data," Harrington discloses a system with a DRDRAM which is connected to a memory device to check power operational states of specific address in memory. (Lines 57-65 of Column 2). Harrington also discloses that any connector capable of receiving a signal for test can be used to connect the tester to the memory. (Lines 40-48 of Column 5, see also Figure 2).

h. Regarding the limitation of "a test procedure control unit, coupled to the command translation unit and the computer main board for issuing test control commands according to a preset testing procedure and reading the latched write-in data inside the command translation unit so that functionality of the computer main board is assessed and results are registered," Harrington discloses a system in which DRDRAM issues test commands based on stored readable instructions (Lines 25-30 of Column 6). Harrington also discloses that test results are gathered and analyzed by the DRDRAM during testing. (Lines 38-60 of Column 7 and Lines 55-60 of Column 8). Harrington does not disclose a test procedure control unit that can latch write-in data inside the computer main board. Miners discloses a system with a test management logic that accepts test parameter in a configuration register and are transferred from the test controller over the test control bus. (Lines 18-20 of Column 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the

power test circuitry of Harrington with the BIST of Miner. One of ordinary skill would have been inclined because Harrington discloses the need of and external memory-testing device for storing testing procedures. (Lines 5-18 of Column 6). Miner discloses this test management logic external to the system to fulfill the stated need of Harrington. (See Miner figure 5).

i. Regarding the limitation of "test result display unit for displaying the test results," Miner discloses a system with means to display and analysis results from test commands. (Lines 53-60 of Column 11).

j. Regarding the limitation of "selecting the preset testing procedure loop," Harrington discloses a system wherein test instructions can be stored and selected from 3 CAL commands. (Lines 58-60 of Column 6).

k. Regarding the limitation of "wherein the test control command comprises at least one of the following commands: power switching command and reset command," Harrington discloses a system wherein a Standby/reduced power state is tested. (Lines 4-6 of Column 3 and Lines 57-60 of Column 7).

Response to Arguments

24. Applicant's arguments filed 01/05/2006 have been fully considered but they are not persuasive.

25. New claim 21 stands rejected. (See above).

26. Regarding the applicants argues on page 6-10 of the response that the preamble passes the test of Utility and Enablement to have patentable weight. The examiner agrees and withdraws the arguments put forth in the last action.

27. Regarding the arguments over claims 1, 13, and 15 (Page 11 of the response). The examiner disagrees with the applicants assertion that a "BIST can only be characterized as a component / feature as part of a 'computer main board'" (Second paragraph, 4th Line, Page 11). The examiner contends Miner explicitly discloses that the object of the invention in the abstract is "an apparatus and method are provided for test memory circuits in a microprocessor." (Examiner underline added, First line of the abstract of Miner). The applicant further argues that because the BIST is only part of the microprocessor because is does not teach PCI interfaces, ACPI, BIOS, or have a CPU. The examiner contends that Miner could have the potential for these features, (as best shown by figure 5). The figure in shows "connections to normal peripheral circuits." However, the examiner also contends that the features argued for by the applicant are not claimed. If the argued features where claimed, the examiner would be of a different opinion. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., BIST is only part of the microprocessor because is does not teach PCI interfaces, ACPI, BIOS, or have a CPU) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

28. Regarding the argument for claims 4 and 18 (Page 12 of the response). The examiner respectfully disagrees with the applicant's assertion that the examiner has to find every element of the claim. The applicant's claim language does not rise to the level of a proper Markush claim language. (See MPEP section 2173.05(h) and 2111.03). Thereby, the examiner contends that because of the "at least one of" claim language results in the examiner only needing to provide on of the elements in rejection. (Please refer to above rejection for claim 4).

Hereby the rejection is maintained. If the argued features where claimed as the applicant desired, the examiner would be of a different opinion.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

30. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman.**

- The supervisor can be reached on **571-272-3644.**

31. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

33. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100.**

34. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

P.O. Box 1450

Alexandria, VA 22313-1450

Tim Bonura
Examiner
Art Unit 2114

tmb
January 23, 2006

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER